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(54) **Digital phase-locked loop using a numerically-controlled oscillator**

(57) An all digital phase loop (PLL) 100 employs a numerically-controlled oscillator (NCO) 140 which is driven by an up/down counter 130. The NCO comprises a ring oscillator with two ranges of control: fine/medium and coarse. A controller 120 determines when the NCO frequency signal is off from a reference signal and whether phase shift should be taken into account when updating the counter. A synchronization mode of operation is provided to zero out any accumulated phase error every n^{th} cycle.

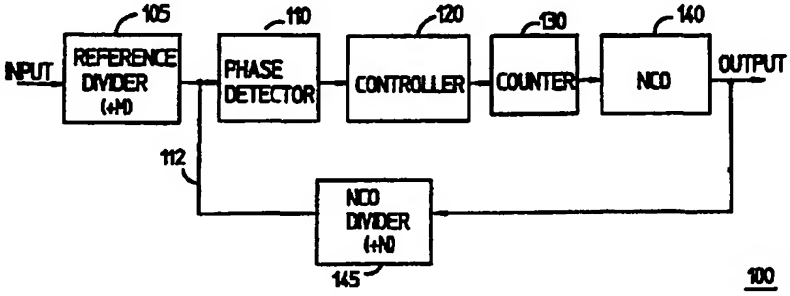


FIG 1

GB 2 288 086 A

The specification as filed includes a computer program which is not reproduced here; it may be inspected in accordance with Section 118 of the Patents Act 1977.

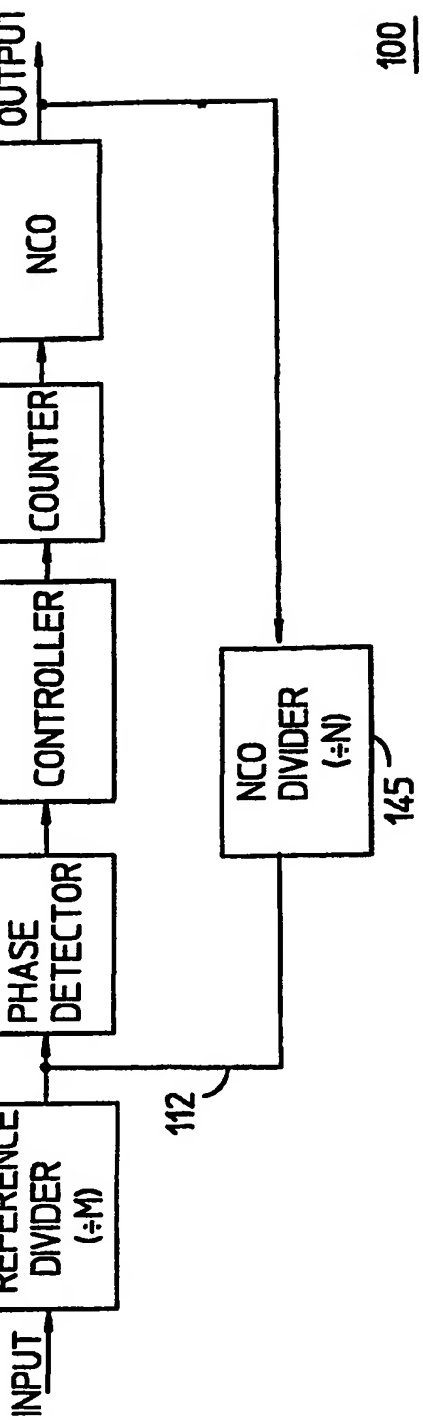

100
INPUT
OUTPUT
105
REFERENCE DIVIDER (÷M)
110
PHASE DETECTOR
120
CONTROLLER
130
COUNTER
140
NCO
112
NCO DIVIDER (÷N)
145

FIG 1

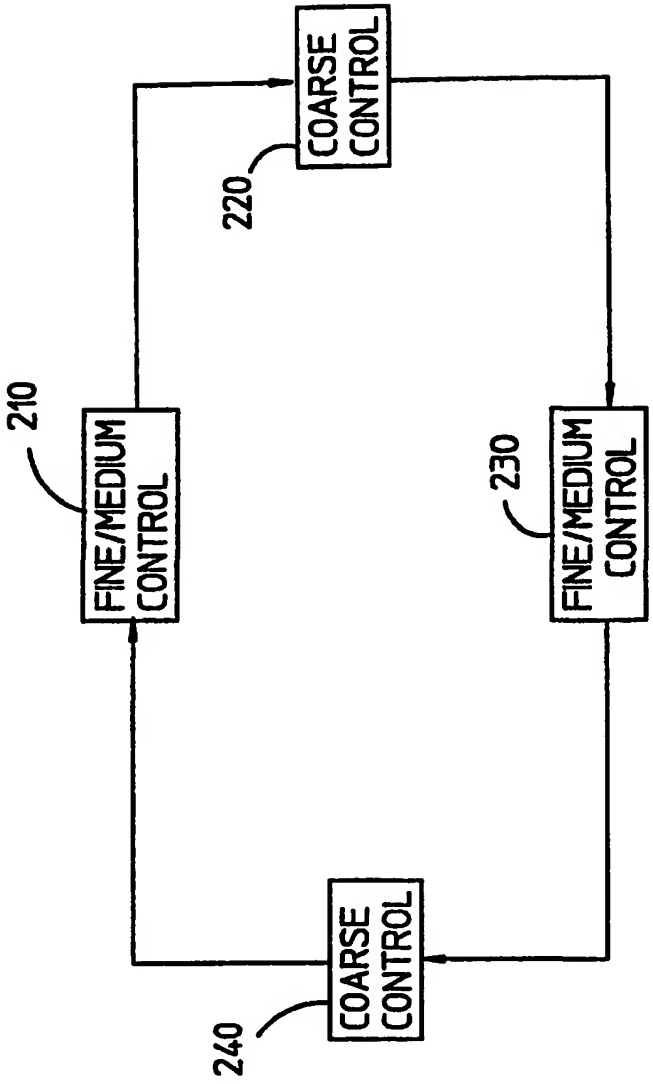

COARSE CONTROL
220
FINE/MEDIUM CONTROL
210
FINE/MEDIUM CONTROL
230
COARSE CONTROL
240

FIG 2

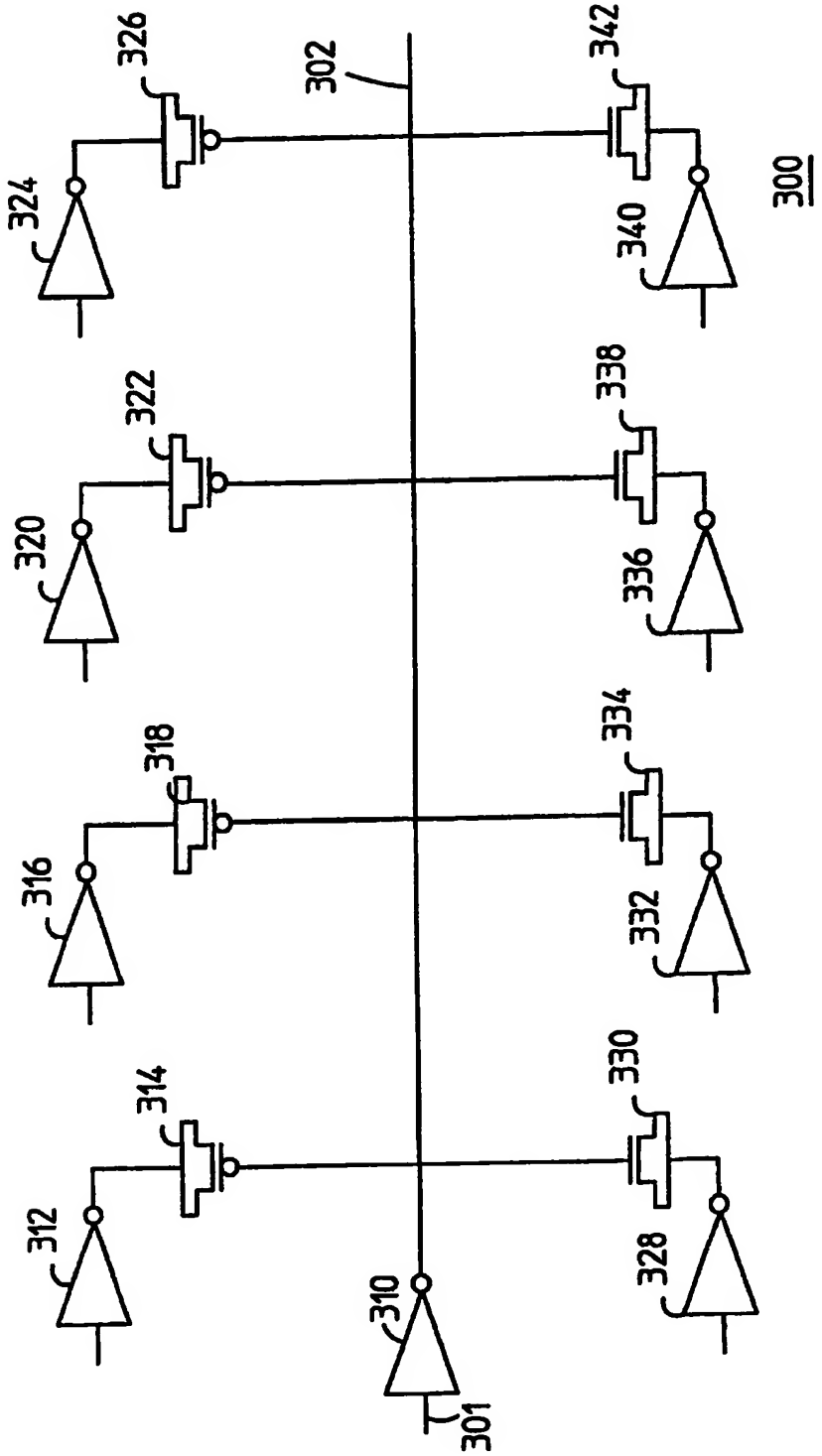

326
302
342
324
340
300
322
338
320
336
318
334
316
332
314
330
312
328
310
301

FIG 3

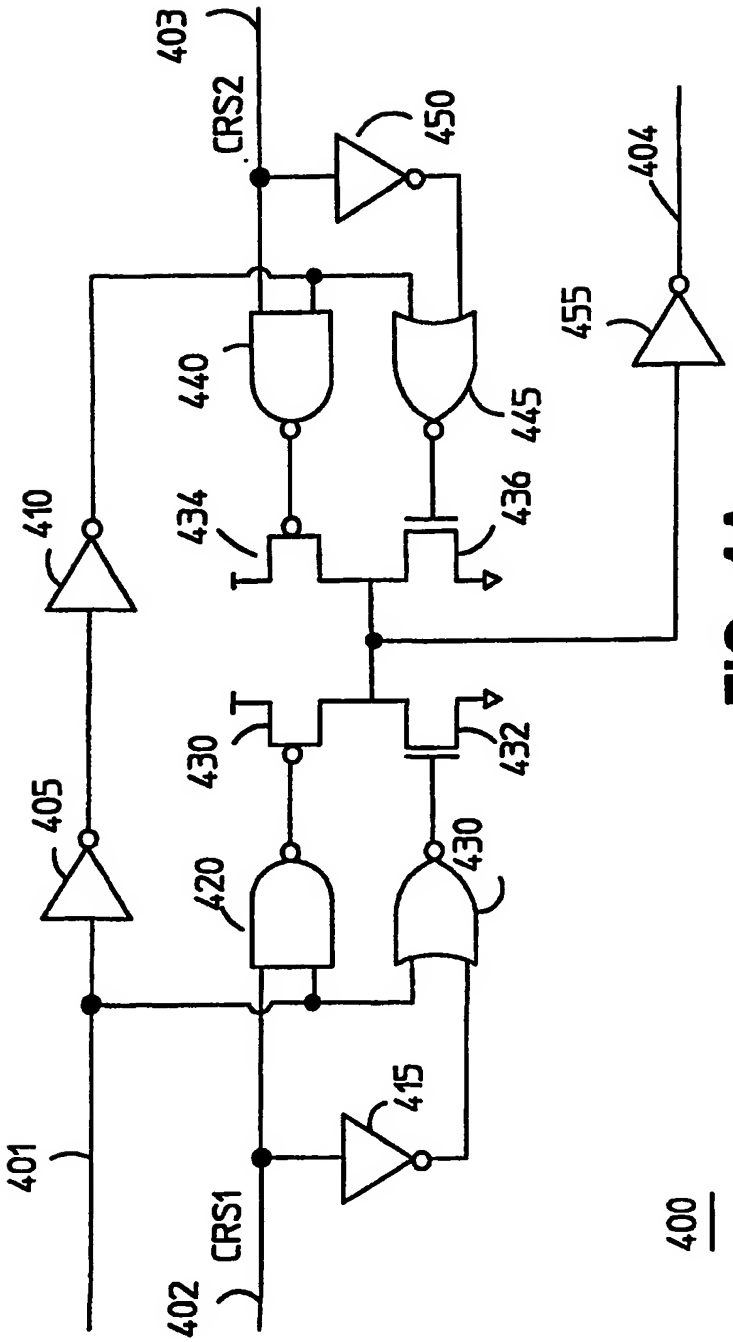
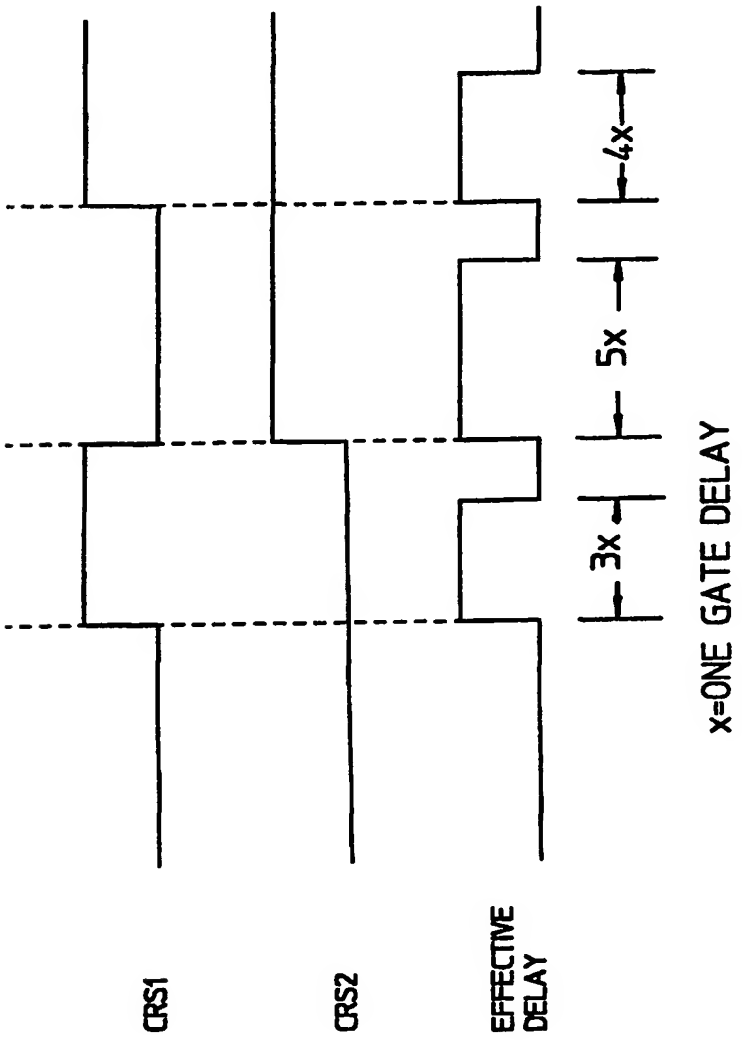

403
CRS2
450
404
455
440
445
410
434
436
430
432
405
420
430
415
401
CRS1
402
400

FIG 4A

FIG 4B



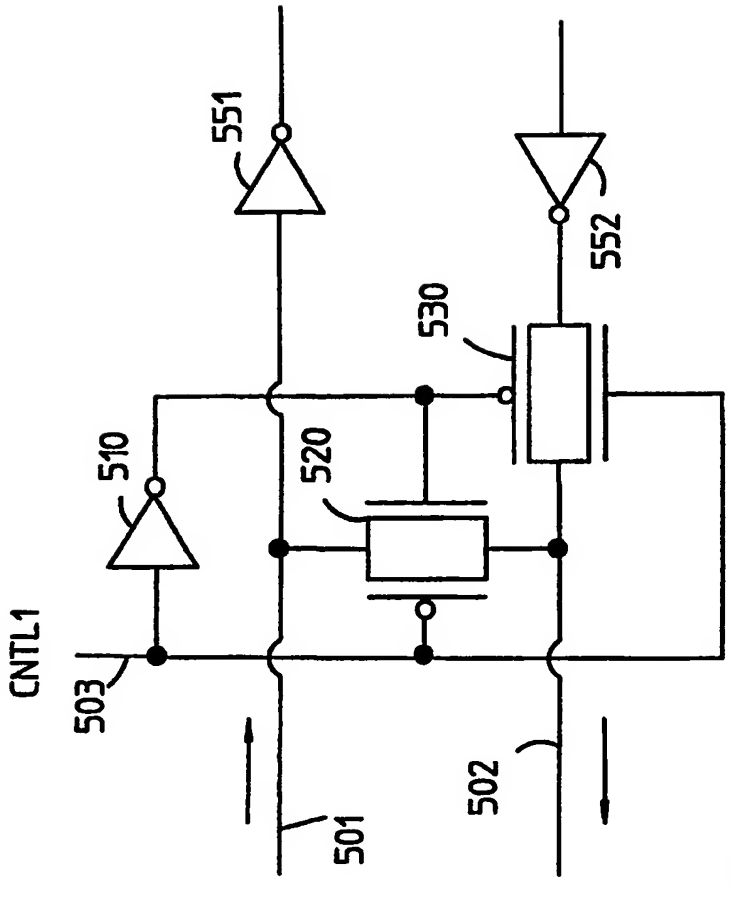


FIG 5A

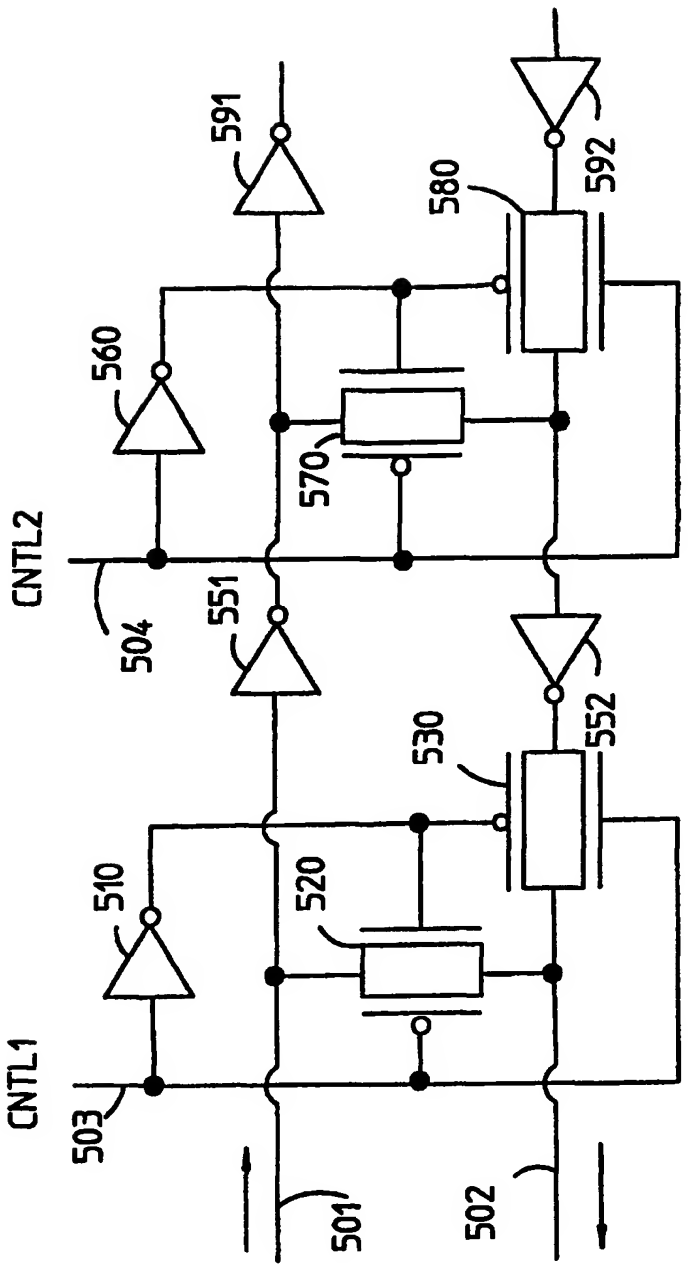

591
592
580
560
570
CNTL2
504
551
552
530
510
520
CNTL1
503
501
502

FIG 5B

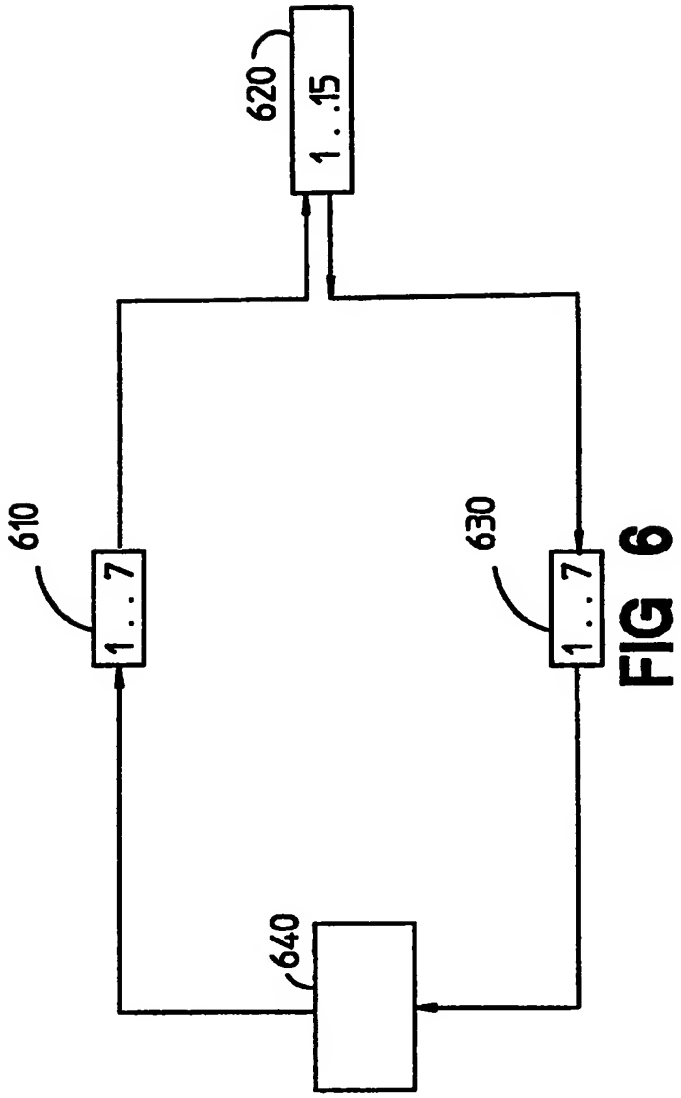


FIG 6

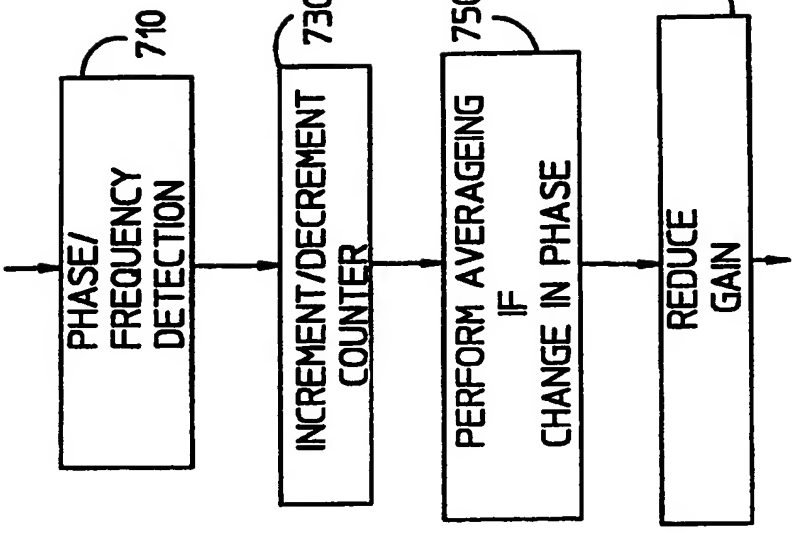

PHASE/
FREQUENCY
DETECTION
710
INCREMENT/DECREMENT
COUNTER
730
PERFORM AVERAGEING
IF
CHANGE IN PHASE
750
REDUCE
GAIN
770

FIG 7

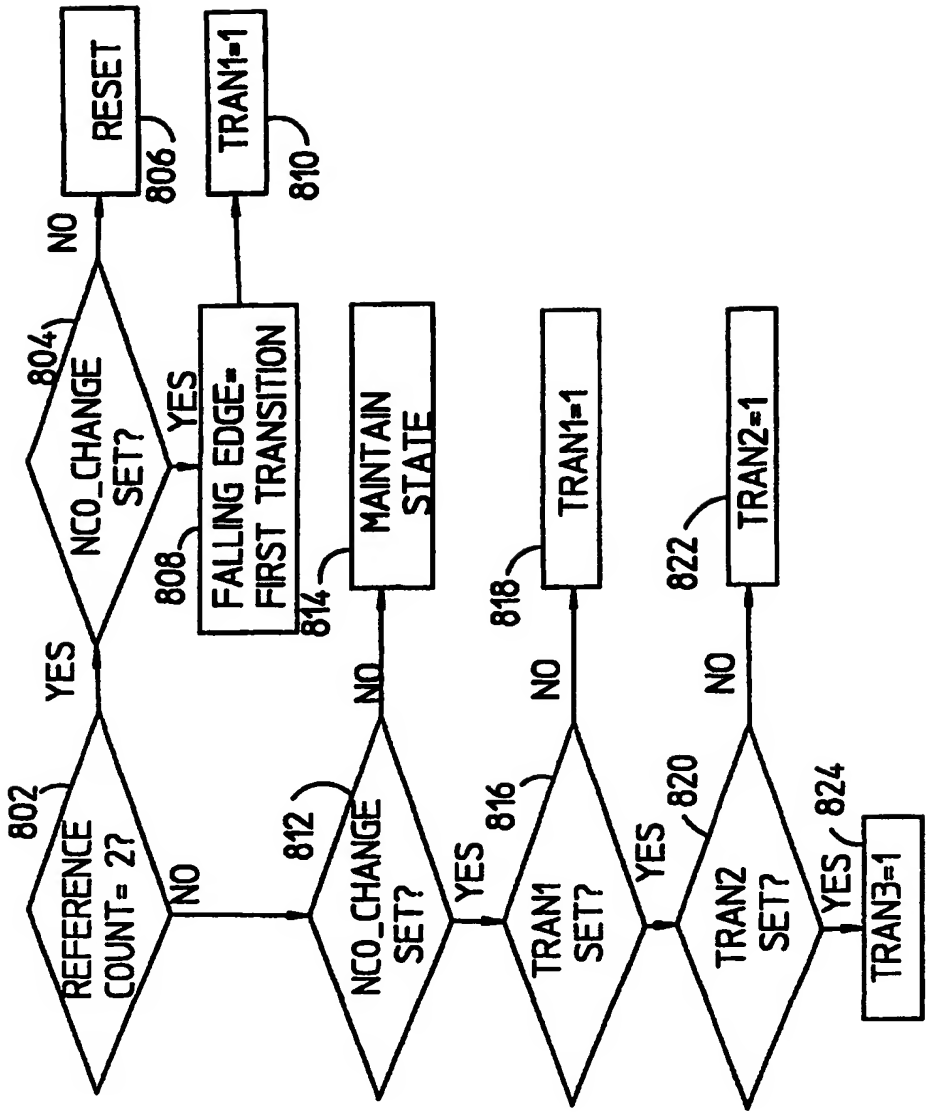

802
REFERENCE COUNT= 2?
YES
NO
804
NCO_CHANGE SET?
NO
YES
806
RESET
808
FALLING EDGE= FIRST TRANSITION
810
TRAN1=1
812
NCO_CHANGE SET?
NO
YES
814
MAINTAIN STATE
816
TRAN1 SET?
NO
YES
818
TRAN1=1
820
TRAN2 SET?
NO
YES
822
TRAN2=1
824
TRAN3=1

FIG 8

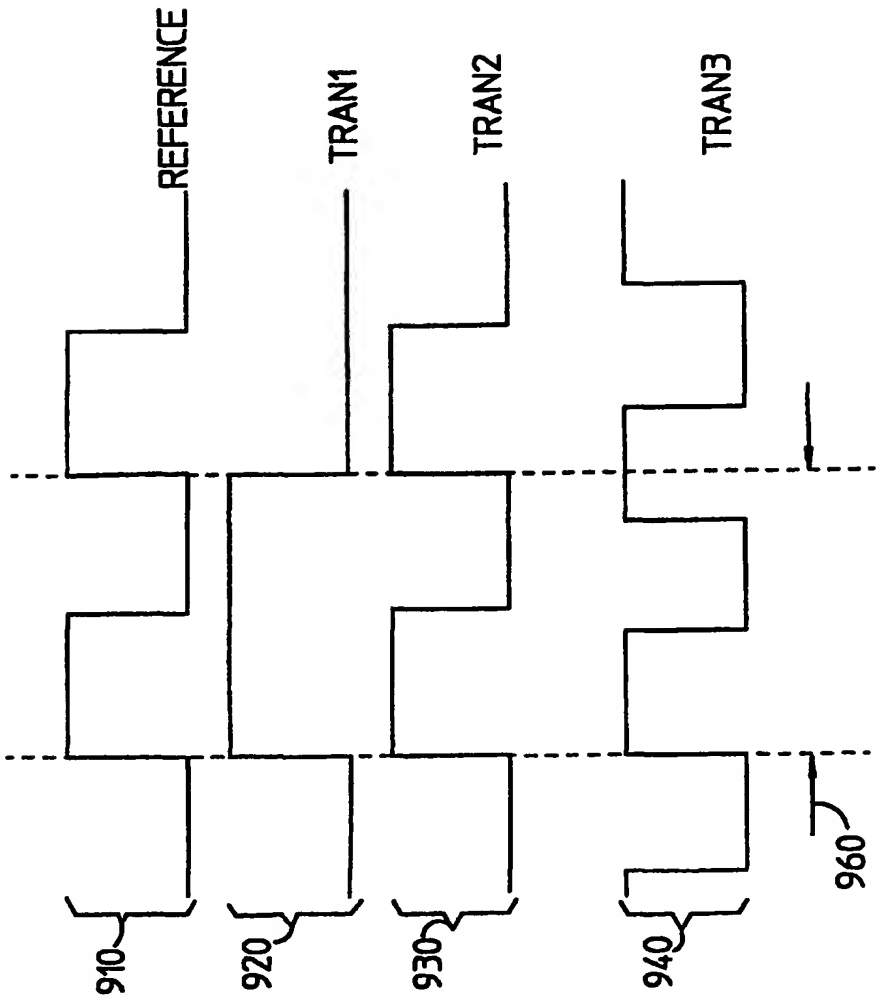


FIG 9

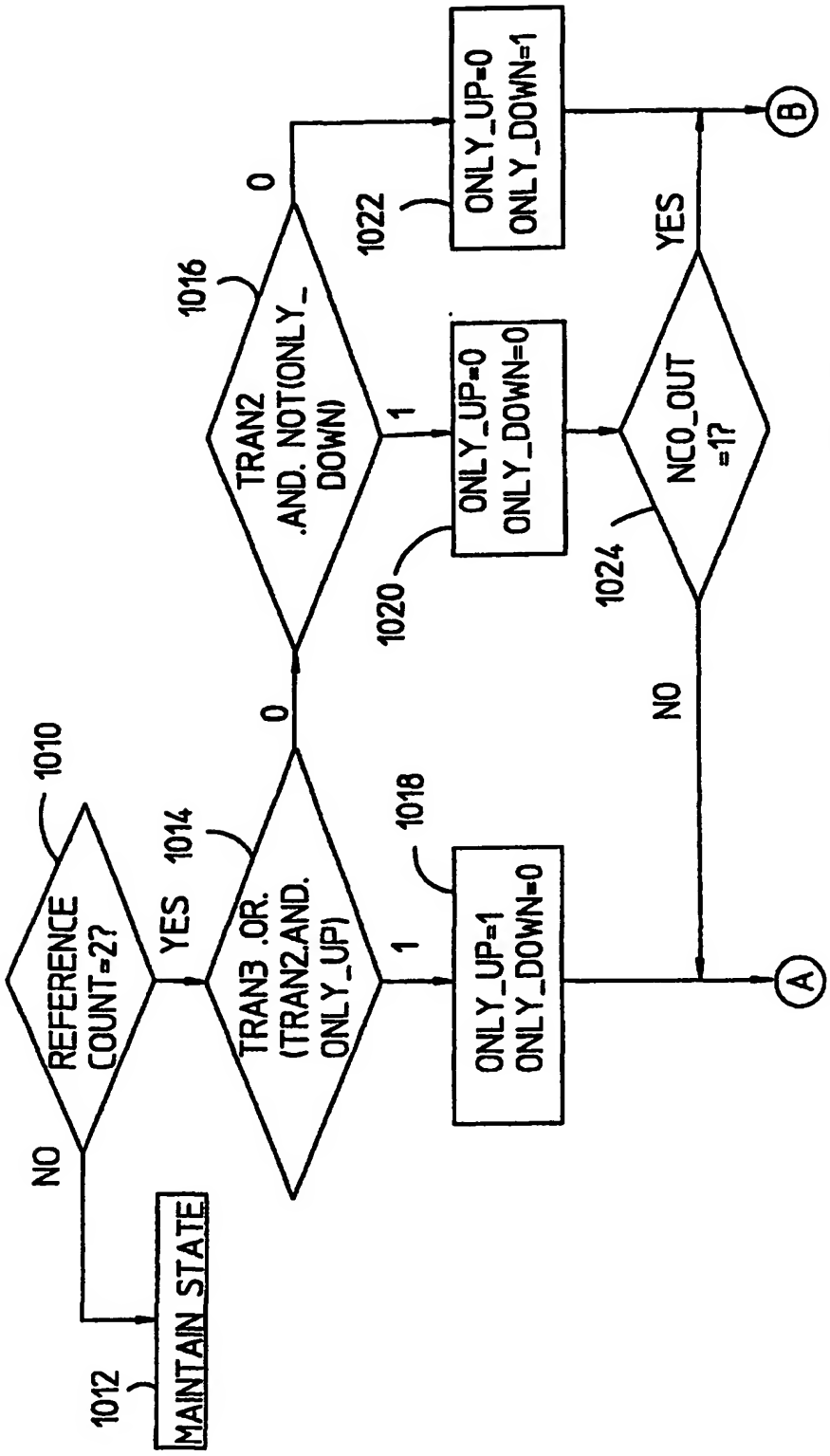

1010
REFERENCE COUNT=2?
NO
YES
1012
MAINTAIN STATE
1014
TRAN3 .OR. (TRAN2.AND. ONLY_UP)
0
1
1018
ONLY_UP=1
ONLY_DOWN=0
1016
TRAN2 .AND. NOT(ONLY_ DOWN)
0
1
1020
ONLY_UP=0
ONLY_DOWN=0
1022
ONLY_UP=0
ONLY_DOWN=1
1024
NCO_OUT =1?
NO
YES
A
B

FIG 10

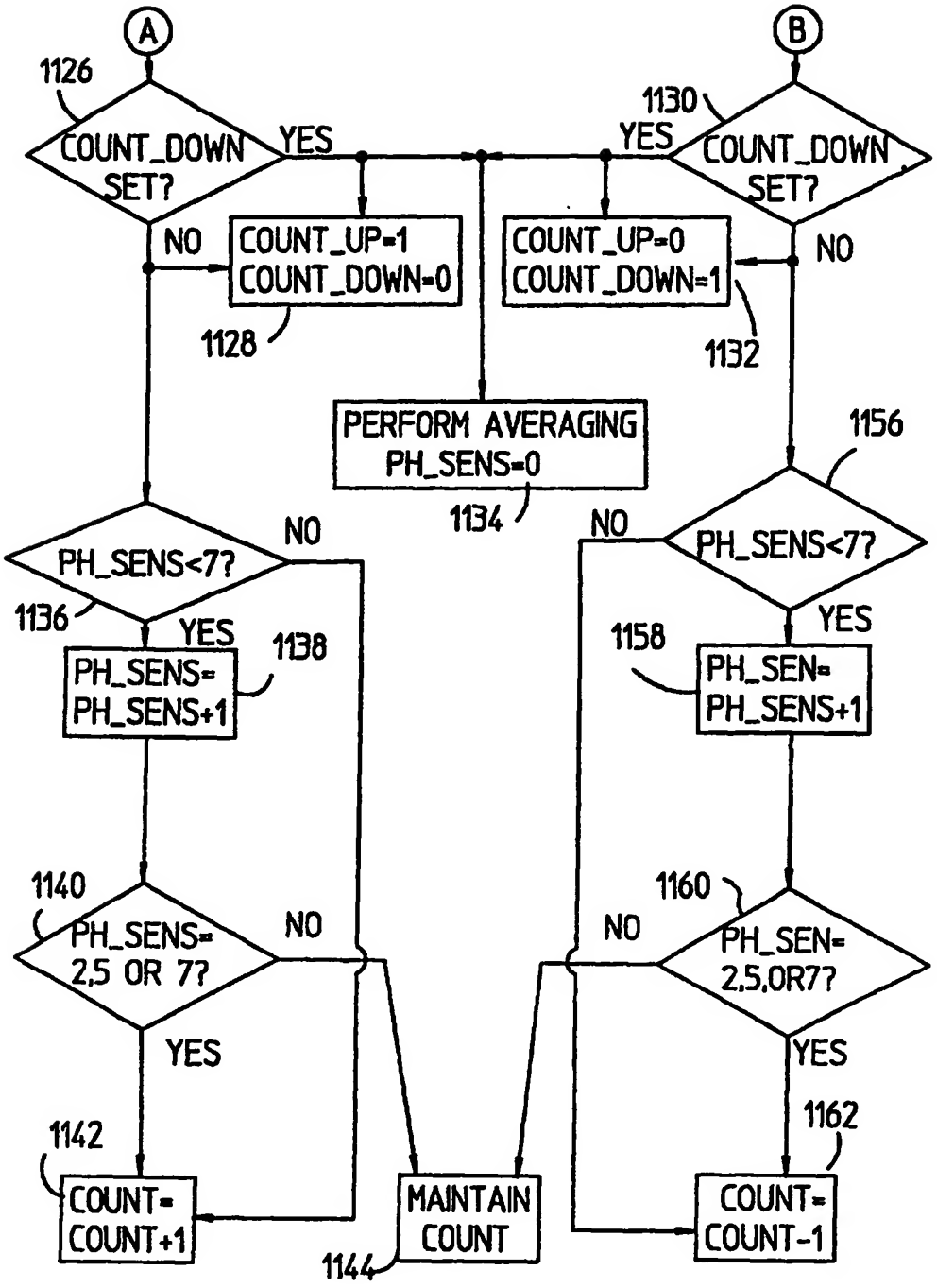

A
B
1126
COUNT_DOWN SET?
YES
NO
COUNT_UP=1
COUNT_DOWN=0
1128
1130
COUNT_DOWN SET?
YES
NO
COUNT_UP=0
COUNT_DOWN=1
1132
PERFORM AVERAGING
PH_SENS=0
1134
PH_SENS<7?
NO
1136
YES
PH_SENS=
PH_SENS+1
1138
1140
PH_SENS= 2,5 OR 7?
NO
YES
1142
COUNT=
COUNT+1
1156
PH_SENS<7?
NO
YES
1158
PH_SEN=
PH_SENS+1
1160
PH_SEN= 2,5,OR7?
NO
YES
1162
COUNT=
COUNT-1
MAINTAIN COUNT
1144

FIG 11

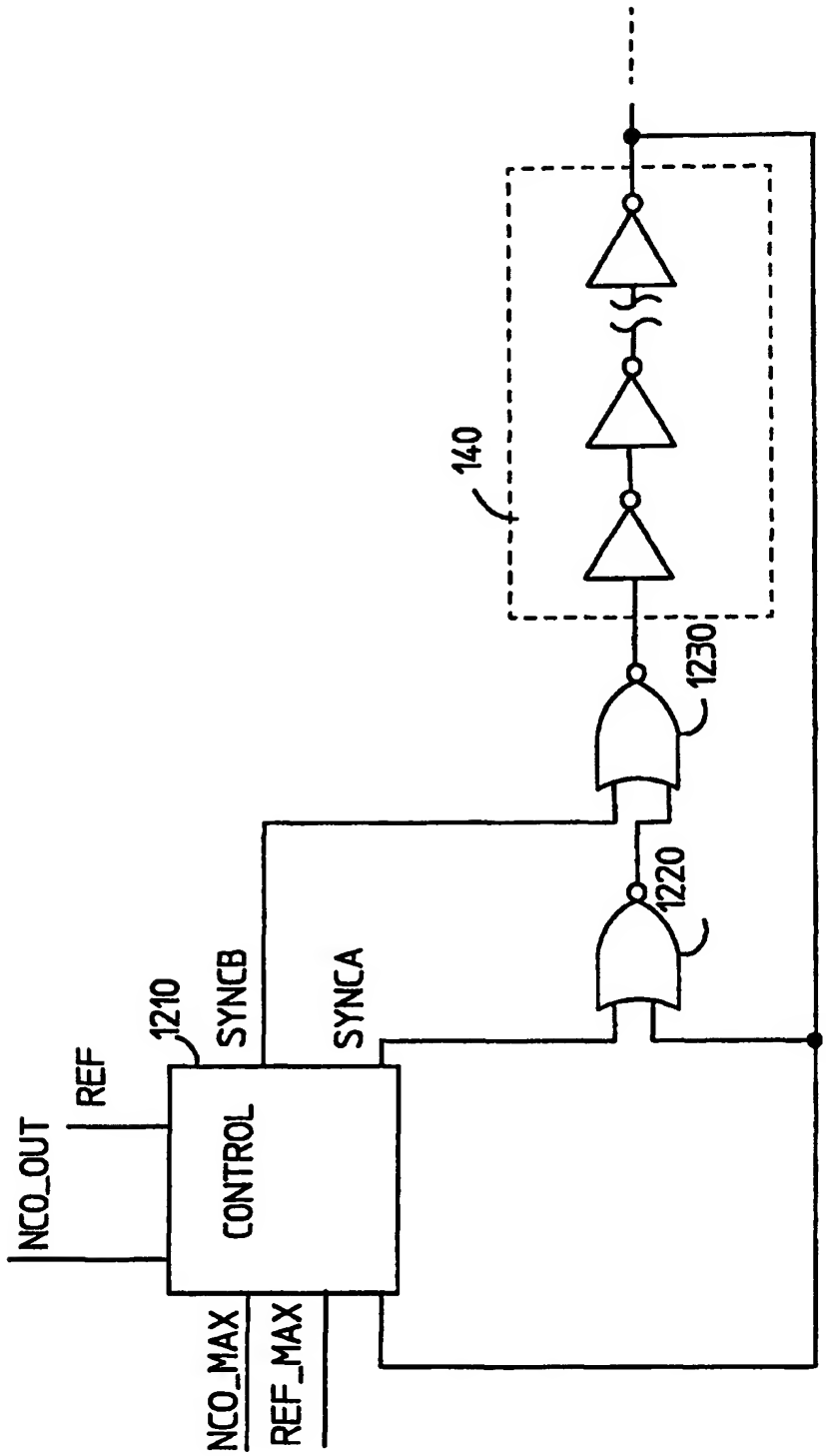

NCO_OUT
REF
1210
CONTROL
SYNCB
SYNCA
NCO_MAX
REF_MAX
1220
1230
140

FIG 12

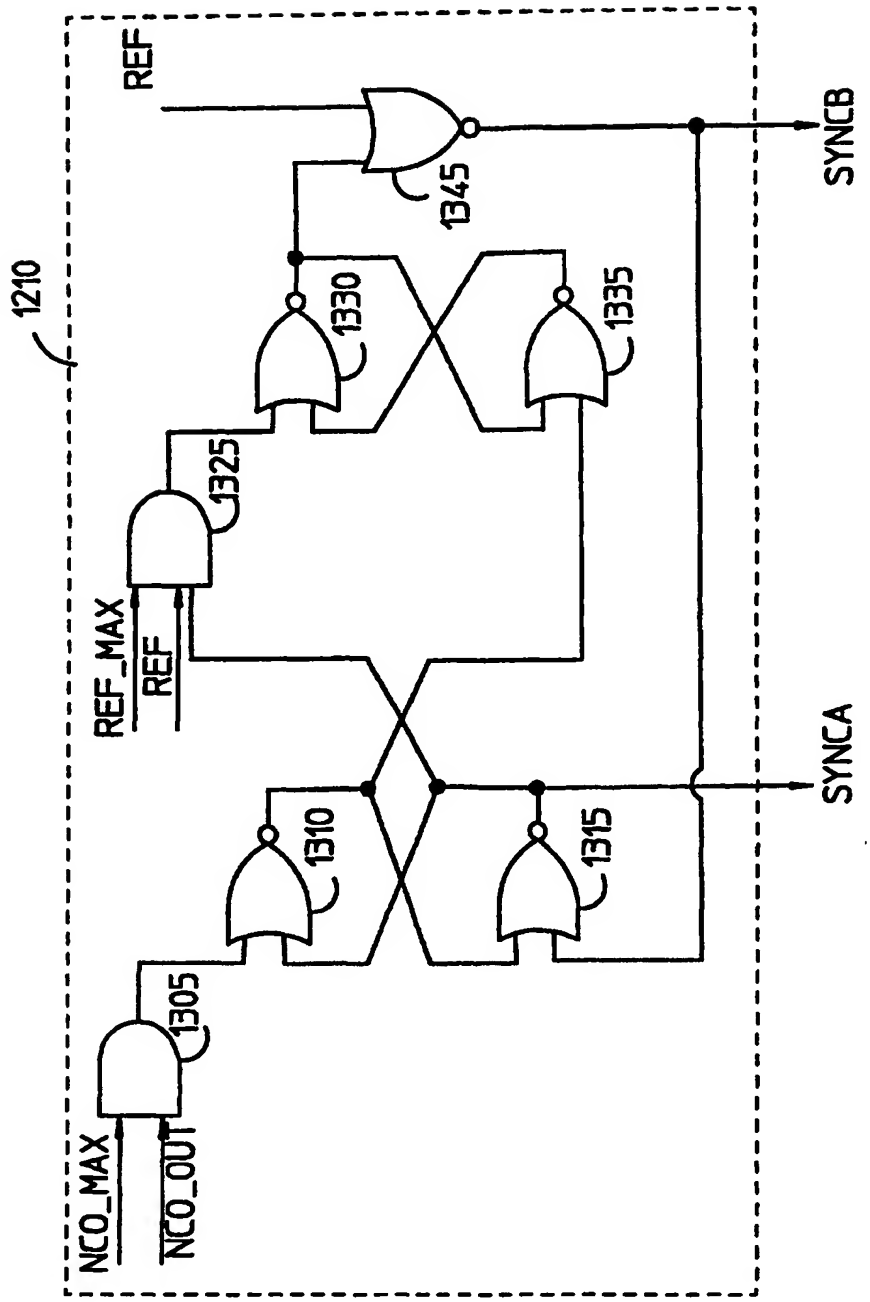

1210
REF
1345
SYNCB
1330
1335
1325
REF_MAX
REF
SYNCA
1310
1315
1305
NCO_MAX
NCO_OUT

FIG 13

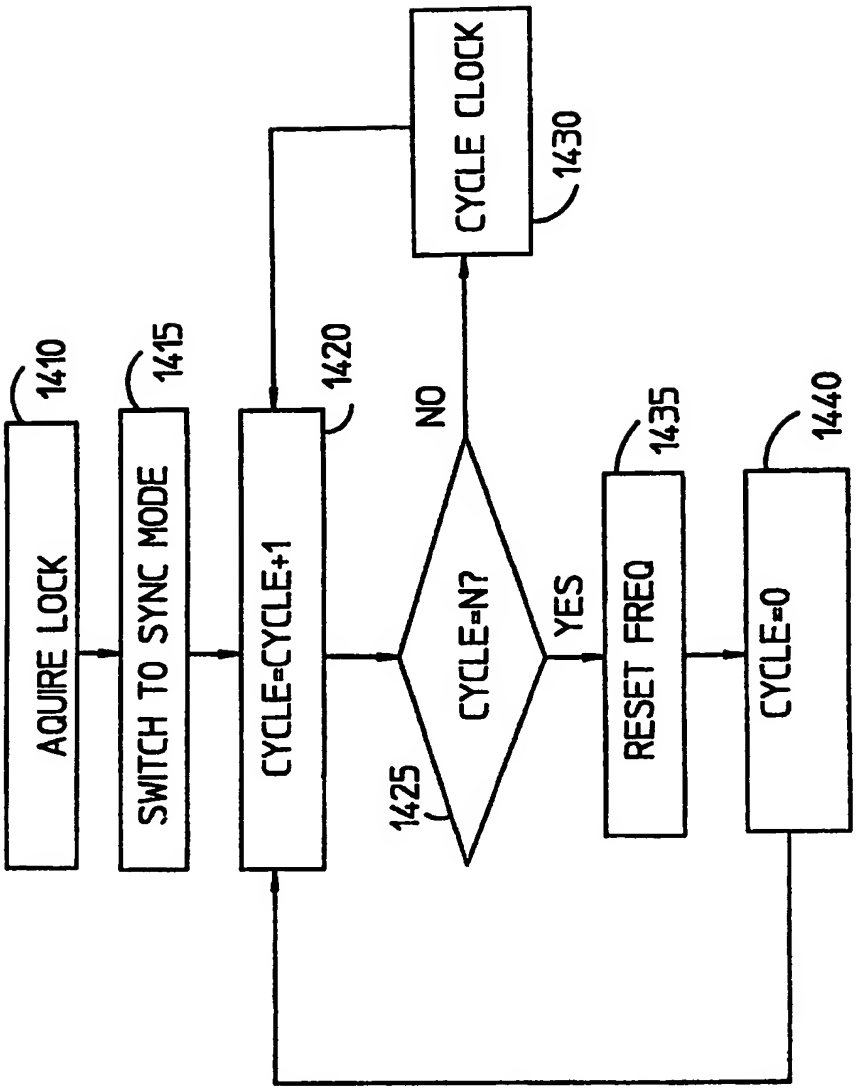

AQUIRE LOCK
1410
SWITCH TO SYNC MODE
1415
CYCLE=CYCLE+1
1420
CYCLE CLOCK
1430
NO
CYCLE=N?
1425
YES
RESET FREQ
1435
CYCLE=0
1440

FIG 14

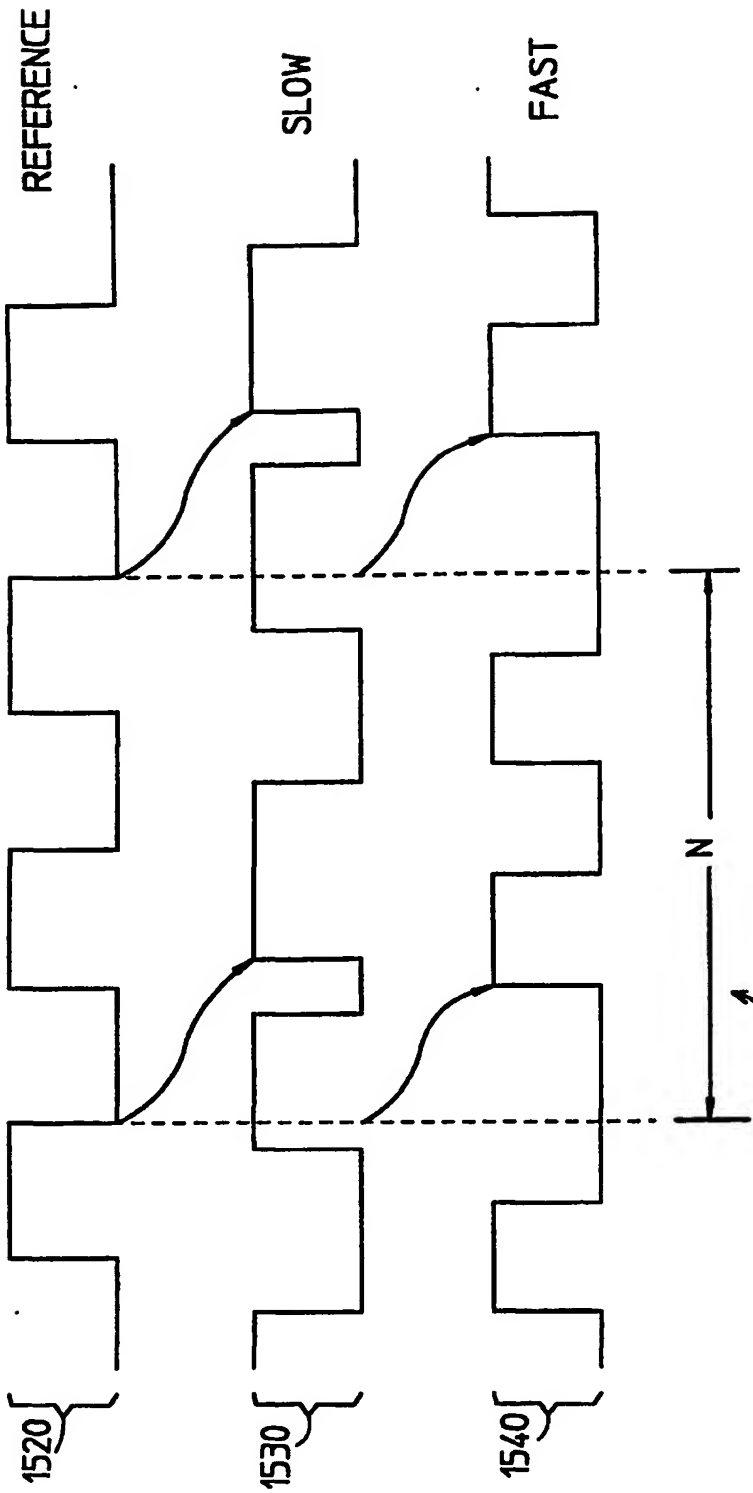


FIG 15

2288086

ALL DIGITAL PHASE-LOCKED LOOP USING A NUMERICALLY-CONTROLLED OSCILLATOR AND A METHOD FOR OPERATING SAME

The present invention relates generally to control systems and more particularly to a digital phase-locked loop employing a numerically-controlled oscillator and counter control logic.

A phased-locked loop (PLL) is a closed-loop control system and a standard building block in circuits containing analog and digital elements. Conventional PLLs contain a phase detector, an oscillator controlled by either a voltage or current source, and a low pass loop filter which connects the output of the phase detector with the input of the oscillator. The loop filter typically employs a large storage capacitor. Two signals are fed into the phase detector: (1) a reference signal, typically a reference frequency; and (2) the output signal from the voltage-controlled oscillator. The phase detector then generates an error signal indicative of

the phase difference between the signals. This phase difference is then converted to a low frequency signal by the loop filter and fed into the oscillator. The PLL is designed so that phase lock eventually occurs between the input reference signal and the generated output signal. PLLs can be used for tone decoding, demodulation of AM and FM signals, frequency multiplication and regeneration of clean signals (i.e., signals relatively free of noise).

The present invention provides an all digital phase-locked loop which employs a numerically-controlled oscillator (NCO). The NCO is driven by an up/down counter which, in conjunction with a controller, controls the period of the NCO. The NCO comprises a ring oscillator with two ranges of control: fine/medium and coarse. Using these two ranges, control blocks add varying amounts of delay to a reference frequency signal. A fine/medium control block employs switched capacitor loads on an output node (also know as an internal node) of an inverter. A coarse control block is essentially constructed using two small coarse control circuits. A first circuit comprises NAND and NOR gate combinations; a second circuit is constructed in stages wherein each stage comprises at least one inverter and a pair of transfer gates. In a preferred embodiment, the NCO comprises 14 fine/medium control blocks for generating approximately a 3 inverter delay, one coarse control circuit for selectively generating 3 to 5 inverter delays, and a coarse control circuit comprising 15 stages, each stage providing a 3 inverter delay.

The controller determines when the NCO frequency is off from the reference and if phase shift should be taken into account when updating the counter. The controller is then used to determine counter updates in terms of direction (i.e., whether to count up or down) and magnitude. The controller is implemented in a state machine that runs at the reference frequency.

A mode of operation for the PLL, known as the synchronization (synch) mode, is provided to zero out accumulated phase error every n^{th} cycle. Running the PLL in synch mode utilizes the reference signal to force a signal edge from the NCO. Control logic is provided in series with the PLL to accomplish this task.

FIG. 1 shows a block diagram of the digital phase-locked loop (PLL) according to the present invention.

FIG. 2 shows a top level block diagram of the numerically-controlled oscillator (NCO) according to the present invention.

FIG. 3 shows a circuit block diagram of the fine/medium control circuit block of the NCO.

FIG. 4 shows a circuit block diagram of the first coarse control block of the NCO.

FIG. 4a shows a timing diagram for FIG. 4.

FIG. 5 shows a circuit block diagram of the second coarse control block of the NCO.

FIG. 5a shows a two-stage second coarse circuit block.

FIG. 6 shows a block diagram of the NCO according to the present invention.

FIG. 7 shows a top level flow diagram of the PLL's counter logic according to the present invention.

FIG. 8 shows a flow diagram of the frequency detection portion of the PLL controller.

FIG. 9 shows a timing diagram indicative of three possible output frequency transitions.

FIG. 10 shows a flow diagram of the counter control portion of the PLL controller.

FIG. 11 shows a flow diagram of the phase sense detection and gain reduction portions of the PLL controller.

FIG. 12 shows a block diagram of the control logic which implements the synchronization mode function of the PLL.

FIG. 13 shows a more detailed block diagram of the control logic seen in FIG. 12.

FIG. 14 shows a flow diagram of a preferred embodiment of PLL operation, including synch mode operation.

FIG. 15 shows a timing diagram of the effect synch mode operation on a slow and a fast oscillator.

An all-digital phase-locked loop (PLL) is presented. The digital PLL is constructed in a similar overall manner to the conventional PLL, except that the individual components that constitute the digital PLL are different. The principle differences are the low-pass loop filter and the oscillator. Instead of implementing the loop filter with resistors, capacitors and an op-amp, the filter in the digital PLL is implemented with a simple up/down counter with associated control logic. The oscillator in the digital PLL is controlled by the digital output of the counter and is therefore called a numerically-controlled oscillator (NCO).

For purposes of the following discussion, the term "high" corresponds to logical 1 (typically 5 volts) while the term "low" corresponds to a logical 0 (typically 0 volts). It should be obvious to one skilled in the art that, depending on circuit configurations, a "high" may correspond to 0 volts while a "low" may correspond to 5 volts. Additionally, flags or variables which are "set" are given the value logical 1. Flags or variables which are "reset" are given the logical value 0.

All Digital Phase-Locked Loop

FIG. 1 shows a block diagram of the digital phase-locked loop according to the present invention. Briefly, the digital phase-locked loop (PLL) 100

is a closed-loop control system for generating a fixed frequency from an input reference frequency. The PLL 100 uses the reference frequency to control the output frequency of an oscillator. Other applications of the PLL 100 include tone decoding, frequency demodulation, and signal recovery.

The digital PLL 100 comprises a reference divider 105, a phase detector 110, a controller 120, a counter 130, a numerically-controlled oscillator (NCO) 140 and an NCO divider 145. An alternate embodiment (not shown) does not require the reference divider 105 nor the NCO divider 145. The reference divider 105 receives a reference input frequency signal and divides it by a predetermined constant M. The divided output is then sent to the phase detector 110. An output frequency signal is sent via a feedback loop 112, through the NCO divider 145 (which divides the frequency by a predetermined constant N) to the phase detector 110 for comparison with the divided reference frequency signal. The phase detector 110 will determine whether there are any frequency or phase errors present and send this information to the controller 120. One function of the controller 120 is to decide whether to increment or decrement the counter 130 based upon the frequency/phase error output from the phase detector 110. The NCO 140 is implemented using a ring oscillator having elements that provide three ranges of control: fine, medium and coarse. These control elements add varying amounts of delay to the reference frequency signal. The controller 120, in conjunction with the counter 130, regulates these three ranges via regulation of the amount of delay placed upon the reference frequency signal. When the PLL 100 has achieved steady state, the output frequency

will be equal to the reference frequency times N divided by M. A reset mechanism (not shown) can be employed to reset the NCO to a predetermined value.

FIG. 2 shows a top level block diagram of the numerically-controlled oscillator (NCO). The NCO is essentially a ring oscillator that comprises two fine/medium control blocks 210,230 and two coarse control blocks 220, 240. The NCO is one of the primary components of the digital phase-locked loop. In general, control of the NCO is effected by changing the delay through the NCO. The fine/medium control blocks 210,230 regulate switched capacitor loads on the inverters within the ring oscillator. The coarse control blocks 220,240 utilize two basic circuits to allow control in increments of single gate delay. The output of coarse control block 240 is the same as the output of the NCO 140 (in FIG. 1). Other output taps may be made to the ring oscillator without departing from the scope of the present invention. For example, the output of the NCO could be tapped at the output of fine/medium control block 210. The overall resolution of the PLL is one picosecond per phase (i.e., two picoseconds per period). In a preferred embodiment, the base period of the NCO is 7.5 nanoseconds with the ability to increase this by approximately 15 nanoseconds.

FIG. 3 shows a circuit block diagram of the fine/medium control block of the NCO. This control block 300 essentially comprises an inverter 310 having an input 301 and eight control elements. Each control element is a field-effect transistor (FET) capacitor (e.g., item 314). A FET capacitor is formed by tying the drain and source electrodes together to form a single node, thus creating a two-terminal

capacitor. In addition to the inverter 310, the fine control block 300 comprises 4 p-channel FET capacitors (314,318,322,326) and four n-channel FET capacitors (330,334,338,342), each tied to the internal node 302. There are eight inverters, each being connected to a drain/source node of the eight capacitors. The eight inverters are connected to eight control signals (not shown) which controls the voltage applied to the drain/source nodes. The control signals emanate from the controller (item 120 in FIG. 1).

The fine/medium control block 300 takes advantage of the fact that a FET has sufficient capacitance from gate to channel when the FET is turned on. The following discussion will address operation of n-channel FETs. It will be understood by those skilled in the art that p-channel FETs operate in a similar manner, only with different polarity. Switching the logic level on the drain/source node will cause the drain/source voltage to exceed the threshold voltage, thus forming a capacitive channel for an n-channel FET. If the drain/source node is biased high, the gate to source voltage will be negative, effectively keeping the channel in an off mode. When the drain/source voltage is then brought low, the gate voltage will reach the threshold voltage (i.e., approximately 1 volt) and the channel will switch to an on mode. In this state, a large capacitance is formed from gate to channel. Note well that for a p-channel FET, the voltages are reversed. By controlling the voltage on the drain/source node, the capacitance seen by the internal node 302 can be controlled. Increasing the net load on the internal node 302 is accomplished by controlling the voltage to the eight FET capacitors, effectively delaying the output.

In a preferred embodiment, the n-channel FET capacitors occupy an area of 1.2 μm x 1.4 μm and are 0.002 picofarads (pF), or 2 femtofarads (fF); these fine control delay elements each provide a delay of approximately 1 picosecond. The p-channel FET capacitors occupy an area of 6.2 μm x 2.2 μm and are .02 pF, 20 fF; these medium control elements each provide a delay of approximately 10 picoseconds. Other sized capacitors may be used, creating varying delays.

FIG. 4 shows a circuit block diagram of the first coarse control block of the NCO. Three possible delta delays can be generated using this circuit-- three, four and five gate delays. A selector (not shown) determines which delay will be selected. This is accomplished using two control lines, CRS1 402 and CRS2 403. CRS1 402 and CRS2 403 emanate from the controller (item 120 in FIG. 1). When CRS1 402 is high and CRS2 403 is low, a three gate delay is created. When CRS1 402 is low and CRS2 403 is high, a five gate delay is created. Driving both CRS1 402 and CRS2 403 high will effectively create a four gate delay. This occurs because both sides of the circuit are allowed to "drive fight" against each other causing the output delay to be the average of the two delays.

The first coarse circuit block 400 essentially comprises two sub-circuits containing a NAND gate and NOR gate combination; the two sub-circuits are separated by a block of FET switches. Each NAND gate and NOR gate comprise first and second inputs and an output. An input signal 401 is connected to the second input to a first NAND gate 420 and the first input to a first NOR gate 430. The input signal is also connected to the input of the first of a pair of inverters 405,410. After

passing through both inverters 405,410 this signal is then fed to the second NAND/NOR combination, being tied to the second input of a second NAND gate 440 and the first input of a second NOR gate 445. The control signal CRS1 402 is tied to the first input of the first NAND gate 420. CRS1 402 is also passed through an inverter 415 to the second input of the NOR 430. The output of the NAND 420 is connected to the gate of a p-channel FET 430. The output of the NOR 430 is connected to the gate of an n-channel FET 432. The drain electrode of FET 430 is tied to VDD, which is nominally 5 volts. The source of FET 430 is connected to the drain of FET 432. The source electrode of FET 432 is tied to ground, nominally 0 volts.

The second NAND/NOR combination is constructed in a similar manner to the first combination circuit. The control signal CRS2 403 is tied to the first input of the second NAND gate 440. CRS1 403 is also passed through an inverter 450 to the second input of the NOR 445. The output of the NAND 440 is connected to the gate of a p-channel FET 434. The output of the NOR 445 is connected to the gate of an n-channel FET 436. The drain electrode of FET 434 is tied to VDD, which is nominally 5 volts. The source of FET 434 is connected to the drain of FET 436. The source electrode of FET 436 is tied to ground, nominally 0 volts. The output 404 is taken from the FETs 430,432,434,436 and is inverted by inverter 455.

FIG. 5 shows a circuit block diagram of the second coarse control block of the NCO. This second coarse circuit block 500 has been designed so that

multiple stages may be added to effect a ladder-like circuit wherein each step represents an additional delay (see FIG. 5a). The second coarse circuit block 500 comprises three inverters 510,551,552 and two FET transfer gates 520,530. A transfer gate is created using two FETs, one p-channel and one n-channel, wherein the drain electrodes and source electrodes are connected together respectively.

An input signal 501 is connected to transfer gate 520. A control signal, CNTL1, 503 is connected to the p-channel FET of transfer gate 520 and, through inverter 510, the n-channel FET of gate 520. When transfer gate 520 is turned on, the input signal 401 is passed through the gate 520 to the output line 502, providing approximately one inverter gate of delay. While a transfer gate approximates only 1/2 of an inverter gate delay, the additional transfer gate 530 adds an additional load on the output line 502 creating the effective one full inverter gate delay. Inverters 551 and 552 are used to drive to the next subsequent stage and to receive from the subsequent stage (see FIG. 5a). After the signal is delayed by a predetermined number of stages, it returns via path 502. In a preferred embodiment, a gate delay is approximately 175 picoseconds. Other gate delays can be accomplished by modifying circuit layout and other such techniques that are understood by those skilled in the art.

FIG. 5a shows a two-stage coarse control circuit. Depending upon the value of the control signals 503,504, the input signal 501 can go through either: (1) one transfer gate 520; or (2) two inverters (items 551 and 552) and two transfer gates (items 570 and 530). The second configuration will approximate a delay of four

inverters, or an additional three inverters of delay. In a preferred embodiment there are fifteen stages. It will be understood by those in the art that multiple stages can be implemented for this second control circuit by simply adding successive stages; this will provide varying amounts of delays.

FIG. 6 shows a block diagram of the NCO according to the present invention. The preferred embodiment NCO comprises 14 fine/medium control blocks, one coarse control block for 3-5 inverter delays and 15 coarse control blocks for three inverter delays. Blocks 610 and 630 represent the fine/medium control blocks (these are the same as item 300 in FIG. 3). Internally, the 7 fine/medium control blocks are connected in series so that, for example, the internal node (item 302 in FIG. 3) of a first block is connected to the input (item 301 in FIG. 3) of the second block and so on. Block 620 represents the three-inverter-delay blocks (item 500 in FIG. 5). Block 620 is constructed by using 15 three-inverter-delay blocks are connected in ladder-like configuration (as suggested in FIG. 5a). Block 640 represents the 3-5 inverter delay block (item 400 in FIG. 4).

Thus, to connect the various control blocks in FIG. 6 using the control blocks in figures 3, 4 and 5, item 302 (of the last fine/medium control block in block 610) is connected to item 501 (in block 620). Item 502 is connected to item 301 (of the first fine/medium control block in block 630). Item 302 (of the last fine/medium control block in block 630) is connected to item 410 (in block 640) and item 404 is connected to item 301 (of the first fine/medium control block in block 610). The input to the NCO (item 140 in FIG. 1) is essentially the control signals of the various

control blocks (see FIGs. 2-5a). This configuration provides 57 fine steps (0-56 capacitors), 57 medium steps (0-56 capacitors) and 48 coarse steps. Table 1 lists the approximate time steps available from each range.

Step Size	Time Step (in picoseconds)
Fine Step	2
Medium Step	32
Coarse Step	360

Table 1 -- Time Step Delays Within the Numerically-Controlled Oscillator

The PLL Controller

FIG. 7 shows a top level flow diagram of the controller logic according to the present invention. Briefly, the controller (item 120 in FIG. 1) determines the counter updates in terms of direction (count up or count down) and magnitude. The controller also determines when the NCO frequency is off from the reference input frequency and whether the frequency error or phase error should be taken into account when updating the counter. The controller is implemented in a state machine that runs at the reference frequency. In a preferred embodiment the controller, along with the rest of the PLL elements, is implemented in VERILOG, a digital logic simulation system, available from Cadence Design Systems, Two Lowell Research Center Drive, Lowell, Massachusetts. Using the VERILOG Hardware Description

Language, the complete logic layout of the PLL is created; this listing is then fed into SYNOPSYS which essentially builds the logic gates of the PLL controller of the present invention. SYNOPSYS is available from SYNOPSYS, Incorporated, 700 East Middlefield Road, Mountain View, California. The actual model for the present PLL is listed in Appendix A.

Now referring to FIG. 7, the controller cycles through this top level flow diagram every reference clock cycle. The basic idea underlying the controller is to maintain a steady NCO output frequency, based upon the reference input frequency. The controller performs a division on the reference frequency by maintaining a counter. This counter is incremented over a range from 0 to N-1, N being a predetermined reference divide count. In a preferred embodiment, N is programmable with values from 4 to 255. Every N clock cycles the controller must decide whether to modify the output frequency or maintain a steady state. Block 710 determines the output frequency of the NCO and sets a transition flag based upon whether the output frequency is slower, faster, or the same as the reference frequency. If the frequency is the same, then the phase of the NCO is checked against the phase of the reference signal. Based upon the frequency or phase error, block 730 will determine the direction the counter should go in order to bring the output frequency signal into lock with the reference frequency signal. Block 750 will perform an averaging function (discussed more fully below with respect to FIG. 11) if the frequency/phase error changes direction. Block 770 reduces the overall jitter of the NCO frequency by ignoring some of the increment/decrement commands from

block 730 after a phase change is detected. Block 770 will increment the counter if the output frequency is faster than the reference frequency or if the output signal's phase leads the reference signal's phase. Block 770 will decrement the counter if the output frequency is slower than the reference frequency or if the output signal's phase lags the reference signal's phase.

The input to the control block is the signal NCO_OUT. This is the result of sampling the output of the NCO divider (item 145 in FIG. 1) by the reference clock, then delaying it two states with flip-flops (not shown) triggered by the reference clock. This is done to synchronize the NCO's divider output to the reference clock domain and to provide resolving time to minimize any meta-stability of this signal. Every reference clock pulse, the value of NCO_OUT is compared to the last value of NCO_OUT, and if it has changed, the NCO_CHANGE flag is set (i.e., equal to logical "1"), otherwise it is reset.

FIG. 8 shows a flow diagram of the frequency detection portion of the PLL controller. Starting at decisional block 802, the controller determines whether the reference count, the value of the reference counter, is equal to 2. This is because there are two states of delay from the flip-flop that captures the divided output signal. If the reference count is equal to 2, control is passed to decisional block 804 which determines whether the NCO_CHANGE flag has been set. If the NCO_CHANGE flag has not been set, block 804 passes control to block 806 which resets all transition bits (explain more fully below). If the NCO_CHANGE flag has been set, control is passed to block 808 which accepts the next falling edge of the NCO output frequency

as the first transition, and passes control to block 810 to set TRAN1 flag equal to logical "1."

If the reference count is not equal to 2, decisional block 802 passes control to decisional block 812 which determines whether the NCO_CHANGE flag has been set. If the NCO_CHANGE flag has not been set, block 814 maintains the current state of the transition bits. If the NCO_CHANGE flag has been set, control is passed to decisional block 816 to determine whether the TRAN1 flag has been set. The transition bits and associated flags correspond to various states of the NCO output frequency. As is readily seen in FIG. 9, using the period 960 of the reference frequency signal 910, various states of the output frequency signal are illustrated. TRAN1 920 is representative of an output frequency that is slower than the reference frequency, i.e., there is only one "transition" during the reference period 960. TRAN2 930 is representative of an output frequency that is locked with the reference frequency , i.e., there are two transitions and one falling edge. TRAN3 940 is representative of an output frequency that is faster than the reference frequency, i.e., there are three transition, one falling edge and one rising edge during the reference period 960.

Referring back to FIG. 8, if the TRAN1 flag is not set, decisional block 816 will pass control to block 818 to set TRAN1 equal to logical "1." If TRAN1 has already been set, control is passed to decisional block 820 to determine whether TRAN2 has been set. If TRAN2 has not been set, control is passed to block

822 to set TRAN2 equal to logical "1," else control is passed to block 824 to set the TRAN3 flag equal to logical "1."

FIG. 10 shows a flow diagram of the counter control portion of the PLL controller. Starting at decisional block 1010, if the reference count is not equal to 2, control is passed to block 1012 which maintains the present state of the counter. If the reference count is equal to 2, control is passed to decisional block 1014 to determine whether the TRAN3 flag has been set or TRAN2 has been set and the ONLY_UP flag has been set. The ONLY_UP flag and ONLY_DOWN flag are incremental and decremental indicators respectively for the counter based upon a frequency error when the frequency appears to be equal but was just high or low. These flags are reset when the frequency detection changing direction or when a falling edge or when NCO_OUT is detected when the reference count equals 2 or 3. Thus, if the answer for decisional block 1014 is true (i.e., logical "1"), control is passed to block 1018 to set (or refresh) the ONLY_UP flag and reset the ONLY_DOWN flag. Control is then passed to path A which continues in FIG. 11. If decisional block 1014 yields a logical "0," control is passed to decisional block 1016 to determine whether TRAN2 has been set and ONLY_DOWN has not been set. If this is the case, block 1020 resets both ONLY_UP and ONLY_DOWN flags. Otherwise, block 1022 resets ONLY_UP and sets ONLY_DOWN and control is passed to path B which continues in FIG. 11. If block 1020 was visited, control moves through block 1020 to decisional block 1024 which is conditional on the value of NCO_OUT. Thus, the current count is too high when NCO_OUT flag is equal

to logical "1" and too low when NCO_OUT is equal to logical "0." Referring back to decisional block 1024, if NCO_OUT is equal to logical "0," control is passed to path A which continues in FIG. 11. If NCO_OUT is equal to logical "1," control is passed to path B which continues in FIG. 11.

FIG. 11 shows the conclusion of the logical flow of the PLL controller, including the portion detecting phase change and the portion which reduces the gain of the NCO. Entering path A, decisional block 1126 determines whether the COUNT_DOWN flag has been set. A change in phase sense is detected if COUNT_DOWN flag is equal to logical "1," i.e., has been set. If this is the case, control is passed to blocks 1128 and 1134 simultaneously. Block 1128 sets the COUNT_UP flag and resets the COUNT_DOWN flag. Block 1134 performs an averaging function (which will be discussed more fully below) and resets the PH_SENS flag. The PH_SENS flag is a count of how many cycles through the controller have occurred since the last change in phase sense. Thus, since the result of decisional block 1126 was logical "1,' the PH_SENS flag must be reset to indicate that there was a change in phase sense.

If the result of decisional block 1126 is logical "0," i.e., the COUNT_DOWN flag has not been set, control is passed simultaneously to block 1128 and decisional block 1136. Decisional block 1136 determines whether the PH_SENS flag is less than 7. If PH_SENS is equal to or greater than 7, control is passed to block 1142 which increments COUNT. If PH_SENS is indeed less than 7, control is passed to block 1138 which increments PH_SENS by one. Control is then

passed to decisional block 1140 which determines if PH_SENS is equal to 2, 5 or 7. If this proves true, block 1142 receives control to increment COUNT; else control is passed to block 1144 to maintain COUNT at its present state. One reason for incrementing COUNT only when PH_SENS is equal to 2, 5 or 7 is to keep the counter close to an "ideal" count. Since the counter will always be incrementing and decrementing around an ideal count, it would be beneficial to keep within +/- 1. It has been found that it is not necessary to increment or decrement every cycle. Thus, the controller can stop counter updates for some of the cycles (e.g., when PH_SENS equals 1, 3, 4 and 6). Path B is a mirror image of path A except for the fact that COUNT may be decremented at block 1162 (recall that path B is indicative of count being too high).

Referring back to the averaging function performed at block 1134, since the counter (item 130 in FIG. 1) approximates a pure integrator having the desired properties of a low pass filter, unwanted oscillation in frequency will likely occur since the counter is in a feedback loop. Thus, a loss mechanism must be inserted into the counter to dampen out this oscillation. In a preferred embodiment, the PLL performs an averaging function every time the sense of the phase detector (item 110 in FIG. 1) changes. Thus a count is maintained that keeps track of each time the phase sense changes. When a phase change occurs, the present values of the fine/medium control elements (i.e., the values of the fine/medium control elements at count equal to K) are averaged with the values these elements had the last time the phase change occurred (i.e., at count equal to K-1). This average value is then used

by the counter instead of incrementing or decrementing the counter. Hence, when either decisional block 1126 or decisional block 1130 result in a logical "1," control is redirected away from the increment and decrement paths (path A and path B respectively) to block 1134. The averaging function facilitates convergence onto the proper count value, keeping the net oscillations to a minimum.

Synchronization Mode of the PLL

FIG. 12 shows a block diagram of the control logic which implements the synchronization (synch) mode function of the PLL. Briefly, the synch mode utilizes the reference signal to force an edge from the NCO. Synch mode essentially zeroes out the accumulated phase error inherent in the oscillator period at regular intervals. As shown in FIG. 12, two NOR gates 1220,1230 are placed in series with the NCO 140, shown as several inverters in series for simplicity. Control logic 1210 (see FIG. 13) is used to generate the SYNC_A and SYNC_B signals. The first NOR gate 1120 is used as a holdoff, i.e., to keep the falling edge from propagating through the NCO. The second NOR gate 1230 is used to take an inverted version of the reference signal and force a new edge into the NCO. The operation of synch mode will now be discussed with respect to FIGs. 14 and 15.

FIG. 14 shows a flow diagram of a preferred embodiment of PLL operation, including synch mode. When the system is initially started, frequency lock is the first task that must be accomplished, as shown in block 1410. Once lock is acquired, operation is switched to synch mode (block 1415). Once in synch mode,

control is passed to block 1420 which increments a cycle count. Decisional block 1425 determines whether the cycle count has reached a predetermined number, N. If the cycle count has not reached N then control is passed through block 1430, which continues through a cycle of the NCO, and back to block 1420 to increment the cycle count once again. Once the cycle count has reached the predetermined N, control is then passed to block 1435 which "resets" the NCO frequency edge. In other words, the reference edge is forced into the NCO. Block 1440 then resets the cycle count to zero before returning to block 1420. In a preferred embodiment, the predetermined N can be programmed to any value from 4 to 255. Other predetermined values may be selected to achieve predictable results.

Refer now to FIG. 15, which shows a timing diagram of the effect of synch mode operation on a slow and fast oscillator. The dotted lines show the point where the phase comparison between the reference signal 1520 and the NCO frequency. The falling edge of the reference signal 1520 is used to generate the next rising edge of the NCO frequency signal. If the oscillator is running slow (item 1530), then a short falling phase is generated as indicated by the arrow in an attempt to synch with the next rising edge of the reference signal 1520. If the oscillator is running fast (item 1540), then the low phase is extended until the next rising edge of the reference signal 1520. As discussed above with respect to FIG. 14, synch mode operation forces the falling edge of reference frequency into the NCO every N cycles. Thus, every N (item 1510), the NCO will either have its signal forced, as in the case of the NCO running slow, or delayed, as in the case of the NCO running fast.

While the present invention has been illustrated and described in connection with the preferred embodiment, it is not to be limited to the particular structure shown. It should be understood by those skilled in the art that various changes and modifications may be made within the purview of the appended claims without departing from the scope of the invention in its broader aspects.

CLAIMS:

1. A digital phase-locked loop comprising:

a phase detector having a detector input and a detector output;

a controller having a controller input and a controller output, the controller input connected to the detector output;

a counter having a counter input and a counter output, the counter input connected to the controller output; and

an NCO having an NCO input and an NCO output, the NCO input being connected to the counter output, the NCO output being connected to the detector input.

2. The digital phase-locked loop of claim 1, wherein the NCO comprises a fine/medium control block and a coarse control block.

3. The digital phase-locked loop of claim 2, wherein the fine/medium control block comprises:

an internal node;

an inverter having an inverter input and an inverter output, the inverter output connected to the internal node;

a control element having a control input and a control output, the control output connected to the internal node; and

control means, connected to the control input, for controlling a voltage applied to the control element.

4. The digital phase-locked loop of claim 3, wherein the control element comprises a FET capacitor.

5. The digital phase-locked loop of claim 2, wherein the fine/medium control block comprises:

an internal node;

an inverter having an inverter input and an inverter output, the inverter input connected to the counter output, the inverter output connected to the internal node;

first and second control elements, each having an input and an output, the output of each control element being connected to the internal node; and

control means, connected to the input of each control element, for controlling a voltage applied to each control element.

6. The digital phase-locked loop of claim 5, wherein each of the first and second control elements comprises a FET capacitor.

7. The digital phase-locked loop of any of claims 2 to 6, wherein the coarse control block comprises a first coarse circuit and a second coarse circuit, the first coarse circuit comprising a selector for selecting three possible delta delays lasting the equivalent of three, four or five gate delays, the second coarse circuit comprising at least one inverter and first and second transfer gates.

8. A method for controlling an NCO, the NCO resides in a digital phase-locked loop having a counter, the digital phase-locked loop receiving a reference frequency signal, the reference frequency signal having a reference phase, the NCO having an operating frequency signal and a characteristic gain, the operating frequency signal having an operating phase, the method comprising the steps of:

(1) detecting a frequency of the operating frequency signal;

(2) changing the counter if the operating frequency signal is different from the reference frequency signal;

(3) determining whether the operating phase is different from the reference phase;

(4) performing an averaging function if the operating phase is different from the reference phase; and

(5) reducing the characteristic gain of the NCO if the operating phase is different from the reference phase.

9. The method of claim 8, wherein step (4) further comprises the steps of:

(6) maintaining a count indicative of when the operating phase is different from the reference phase;

(7) storing a present value indicative of a fine/medium control element at count = K;

(8) retrieving a past value indicative of the fine/medium control element at count = K-1;

(9) calculating an average of the present value and the past value; and

(10) setting the counter equal to the average.

10. A method of operating a digital phase-locked loop, the digital phase-locked loop receiving a reference frequency signal, the method comprising the steps of:

(1) switching the phase-locked loop to a synch mode;

(2) incrementing a cycle counter;

(3) determining whether the cycle counter is equal to a predetermined number; and

(4) setting, if the cycle counter is equal to the predetermined number, an NCO signal edge equal to the reference signal edge.

11. A digital phase-locked loop substantially as herein described with reference to the accompanying drawings.

12. A method of controlling an NCO substantially as herein described with reference to the accompanying drawings.

13. A method of operating a digital phase-locked loop substantially as herein described with reference to the accompanying drawings.

Patents Act 1977 Examiner's report to the Comptroller under Section 17 (The Search report)	Application number GB 9505123.1
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